REMARKS

In the Final Office Action mailed August 30, 2007 (the "Office Action"), the Examiner rejected claims 1, 2, 5, 6, 8, 9, 13, 14, 17, 18, 21, 22, 24, 26, 28, 29, 32, and 33 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,477,614 to Leddige et al. (the "Leddige patent") in view of U.S. Patent Publication No. 2004/0216018 to Cheung (the "Cheung reference") and further in view of U.S. Patent No. 6,370,601 to Baxter (the "Baxter patent"). The Examiner further rejected claims 7, 12, 23, and 34 under 35 U.S.C. 103(a) as being unpatentable over the Leddige patent in view of the Cheung reference and Baxter patent, and further in view of U.S. Patent No. 6,782,465 to Schmidt (the "Schmidt patent"). Claims 4, 11, 20, and 31 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Leddige patent, the Cheung reference, and the Baxter patent, and further in view of Jones, Throughput Expansion with FET Based Crossbar Switching (the "Jones reference"). Claims 15, 16, 25, and 27, have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Leddige patent, Cheung reference and Baxter patent, and further in view of U.S. Patent Publication No. 2004/0243769 to Frame et al. (the "Frame reference").

An information disclosure statement was submitted on August 21, 2007 (the "IDS"). Applicant requests the Examiner consider the references cited in the Form PTO-1449 of the IDS and provide the attorney of record with a signed and initialed copy of the Form PTO-1449.

Claims 1, 8, 13, and 24 are patentable over the Leddige patent in view of the Cheung reference and further in view of the Baxter patent because the combined teachings of the cited references fail to teach or suggest the combination of limitations as recited by the respective claims.

For example, the combination of the references fail to teach a memory hub having a link interface, at least one memory device interface, and a switch as recited in claims 1, 8, 13, and 24. More specifically, claims 1, 8, 13, and 24, as amended, require each of the at least one memory device interface having a memory controller to be coupled to a respective number of the memory devices, and that one of the at least one memory device interface is operable to at least provide and receive signals specific to the respective number of the memory devices. The Examiner relies on the Leddige patent as disclosing a "switch" that is configured to selectively

couple the link interface and the memory device interface. See the Office Action at page 4. Even assuming the Examiner's characterization is correct in that the Leddige patent indeed discloses a "switch" that is configured to selectively couple the link interface and the memory device interface, Leddige still fails to disclose each and every limitation recited by amended claims 1, 8, 13, and 24.

In particular, Leddige fails to disclose, teach, or suggest a memory hub that includes at least one memory device interface having a memory controller where each of the at least one memory device interface is coupled to a respective number of the memory devices, and where one of the at least one memory device interface is operable to at least provide and receive signals specific to the respective number of the memory devices. The Examiner identifies second and third memory buses 321 and 322 as being analogous to the memory device interface recited in the claims. See the Office Action at pages 4-5. As known, buses are merely conductive signal lines that electrically couple a signal from a first device to at least one other device. Unlike memory buses 321 and 322, the memory device interface of claims 1, 8, 13, and 24 are more than mere conductive signal lines coupling signals from one place to another. The memory device interface includes a memory controller and is operable to generate memory control signals for operating the memory devices.

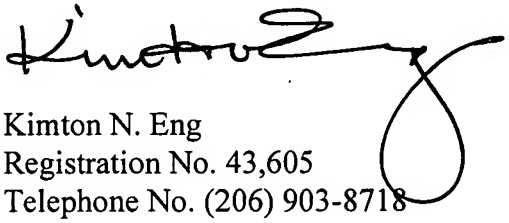
The Examiner has cited the Cheung reference as teaching a DMA controller located on a memory module and cited the Baxter patent as teaching an I/O register operable to store status information. Neither Cheung nor Baxter disclose, teach, or suggest at least one memory device interface as that recited by claims 1, 8, 13, and 24. Therefore, even if it is assumed for the sake of argument that the Examiner's characterization of the Cheung reference and the Baxter patent is accurate, the two references fail to make up for the deficiencies of the Leddige patent.

For the foregoing reasons, claims 1, 8, 13, and 24 are patentable over the Leddige patent in view of the Cheung reference and further in view of the Baxter patent. Claims 2 and 4-7, which depend from claim 1, claims 9, 11, and 12, which depend from claim 8, claims 14-18 and 20-23, which depend from claim 13, and claims 25-29, which depend from claim 24, are similarly patentable based on their dependency from a respective allowable base claim. Therefore, the rejection of claims 1, 2, 4-9, 11-18, and 20-29 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



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